UTM UNIVERSITI TEKNOLOGI MALAYSIA
Sekolah Pendidikan Profesional dan Pendidikan Berterusan (SPACE)

JABATAN KEJURUTERAAN ELEKTRIK
PUSAT PENGAJIAN DIPLOMA (PPD), SPACE
UNIVERSITI TEKNOLOGI MALAYSIA
KUALA LUMPUR

DDWB/E/K 3711
(ELECTRONICS 2)

EXPERIMENT 1
BIPOLAR JUNCTION TRANSISTOR (BJT) AND FIELD EFFECT TRANSISTOR (FET):
AC ANALYSIS

EXPERIMENT 1 : Bipolar Junction Transistor (BJT) and Field Effect Transistor (FET) : AC Analysis

OBJECTIVES

1. To determine the values of voltage gain A_V, input impedance, Z_i and output impedance, Z_o for loaded and unloaded operation in BJT.
2. To determine the values of saturation current, I_{DSS} and pinch off voltage, V_p and the voltage gain, A_v in FET.

COMPONENT/EQUIPMENT

1. Function generator
2. BJT : 2N3904
3. D-MOSFET : DN 2535
4. Oscilloscope
5. Resistor: 1 kΩ (2 units), 3 kΩ (1 unit), 10 kΩ (1 unit), 33 kΩ (1 unit), 1 MΩ (1 unit)
6. Capacitor: 15 µF (2 units), 22 µF (1 unit)

THEORY

Bipolar Junction Transistor (BJT)

The common-emitter (CE) transistor amplifier configuration is widely used. It provides large voltage gain (typically ten to hundred) and provides moderate input and output impedance. The AC signal voltage gain is defined as

$$Av = \frac{Vo}{Vi}$$

where V_i and V_o can both be rms, peak or peak-peak values. The input impedance, Z_i is that of the amplifier (as seen by the input signal). The output impedance, Z_o is that seen looking from the load into the output of the amplifier. The transistor's ac dynamic resistance, r_e, can be calculated using

$$re = \frac{26\, mV}{I_E\, mA}$$

The ac voltage gain of a CE amplifier (under no load / without R_L) can be calculated using

$$A_V = \frac{-R_C}{r_e}$$

The ac input impedance is calculated using

$$Z_i = R_1 // R_2 // \beta r_e$$

(Eq 1)

The ac output impedance is calculated using

$$Z_O = R_C$$

For measurement, the voltage gain is obtained using

$$Av = \frac{Vo}{Vi}$$

For measurement, the transistor's ac dynamic resistance is obtained using

$$r_e = \frac{-R_C}{A}$$

For measurement, the ac input impedance is obtained using

$$Z_i = \frac{V_i}{\left(V_{sig} - V_i\right)} R_X$$

(Eq 2)

For measurement, the ac output impedance is obtained using

$$Z_O = \frac{(V_O - V_L)}{V_L} R_L$$

(Eq 3)

Field Effect Transistor

The common-source (CS) transistor amplifier configuration is widely used.

The AC signal voltage gain is defined as

$$Av = \frac{Vo}{Vi}$$

where V_i and V_o can both be rms, peak or peak-peak values.

The ac voltage gain of a CS amplifier (under no load / without R_L) can be calculated using

$$A_V = -g_m R_D$$

$$g_m = \frac{2I_{DSS}}{V_p} (1 - \frac{V_{GSQ})}{V_P}$$

Part A : BJT : Voltage Gain, Av

<u>Procedures:</u>

1. Make the connections as shown in Figure 1. This arrangement is called Common Emitter Amplifier (CE Amp) that can be represented by block diagram as shown in Figure 2.
2. Apply an AC input signal, V_{sig} = 50 mV_{peak} at frequency, f = I kHz. Observe the output waveform on the oscilloscope to ensure that there is no distortion (if there is distortion, reduce the input signal or check the de bias). CH1 at AC input of circuit and CH2 at AC output of the circuit.
3. Record the resulting DC currents and AC output voltage, Vo in Table 1. Complete Table 1.
4. Sketch the output voltage with reference to the input voltage in the space provided in the answer sheet.

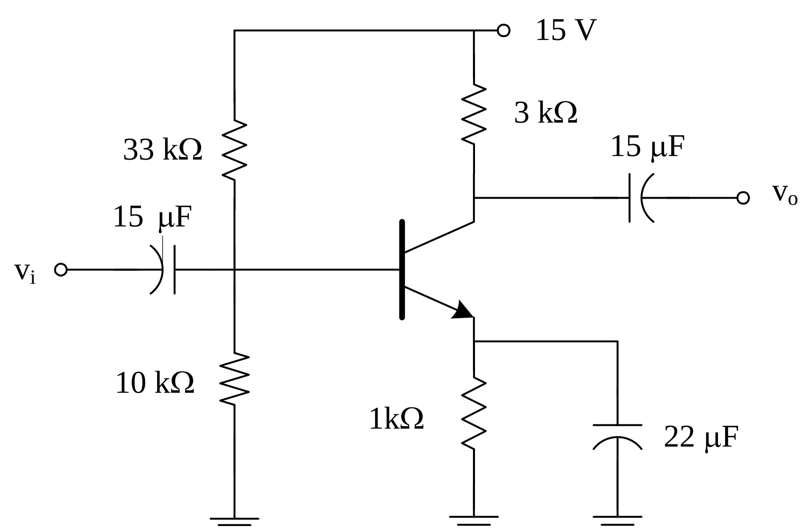


Figure 1

Part B :BJT : Input Impedance, Z_i

Procedures:

1. Connect R_X = 1 kΩ to the CE Amplifier as shown in Figure 2.
2. Apply input signal, V_{sig} = 50 mV_{peak}. Observe the output waveform to ensure that there is no distortion. Measure $V_{i(peak)}$. Record your measurement in Table 2.
3. Using the value of I_C and I_B in Table 2, calculate β.
4. Calculate Z_i using Equation 1 and Equation 2. Show your calculations.

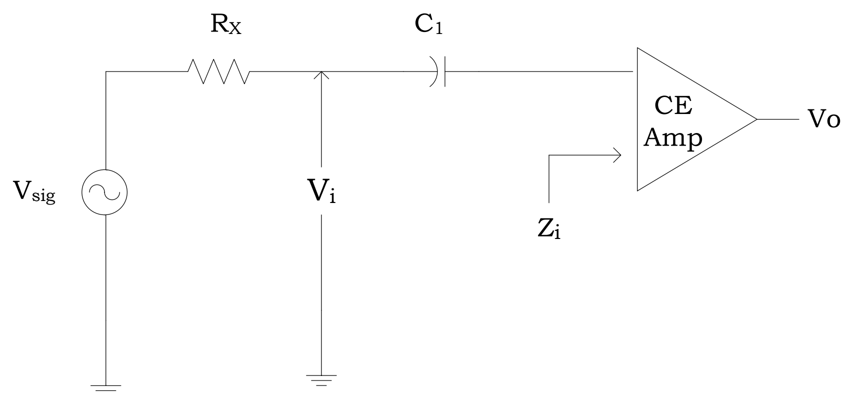


Figure 2

Part C : BJT : Output Impedance, Z_O

Procedures:

1. Remove R_x. Apply input voltage, V_i = 50 $mV_{(peak)}$ and measure the output voltage,$V_{o(peak)}$. Ensure that there is no distortion in output waveform. (This value of V_O is for no load resistor, R_L). Record your measurement in Table 3.
2. Connect load resistor, R_L as shown in Figure 3. Measure $V_{L\ (peak)}$. Record your measurement in Table 4.
3. Complete Table 4. Show your calculations.

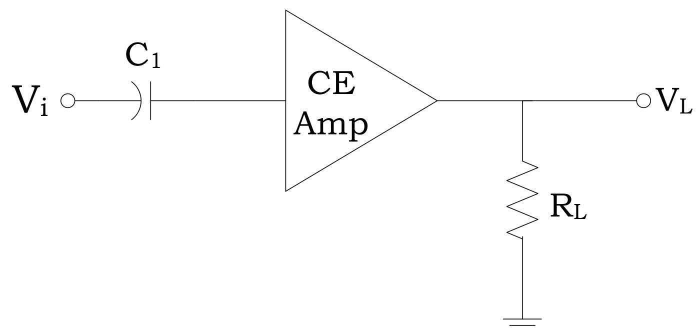


Figure 3

Part D : D-MOSFET : DETERMINATION OF SATURATION CURRENT AND PINCH OFF VOLTAGE

Procedures:

1. Make the connections as shown in Figure 4. Connect the GATE (G) to the negative voltage (V_{GG}) . This negative voltage can be obtained from the Trainer.
2. Set V_{GG} = 0 V. Measure and Record I_D in Table 4. This value is the saturation current I_{DSS}.
3. Varies V_{GG} until I_D =0 mA, Measure and Record V_{GS} in Table 4. This value is pinch off voltage, V_p

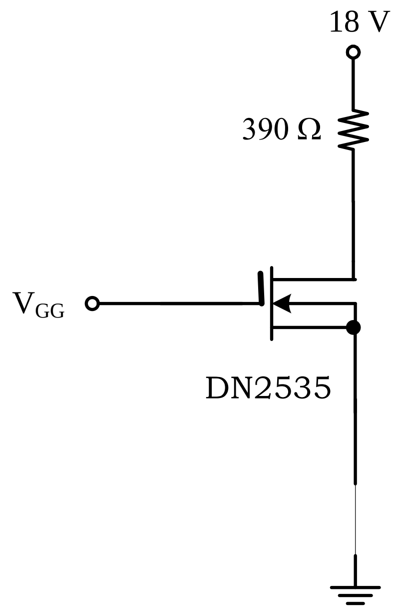


Figure 4

PART E : D-MOSFET : Voltage Gain

Procedures:

1. Make the connections as shown in Figure 5.
2. Measure and record $V_{GS.}$
3. Apply an AC input signal, V_{sig} = 50 mV_{peak} sine wave at frequency, f = I kHz. Observe the output waveform on the oscilloscope to ensure that there is no distortion (if there is distortion, reduce the input signal or check the de bias).
4. Record the resulting DC voltage and AC output voltage, Vo in Table 5. Complete Table 5.
5. Sketch the output voltage with reference to the input voltage in the space provided in the answer sheet.

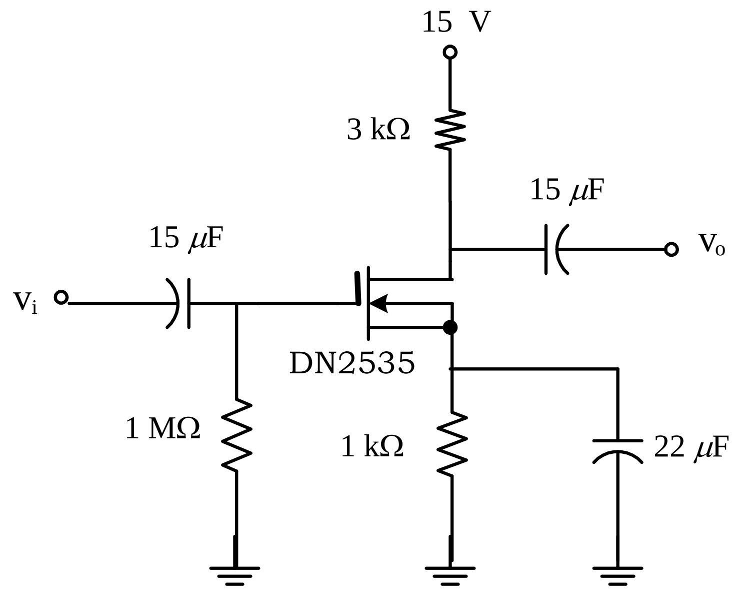


Figure 5.

2N3903, 2N3904

General Purpose Transistors

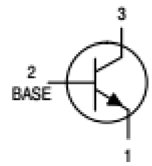
NPN Silicon

Features

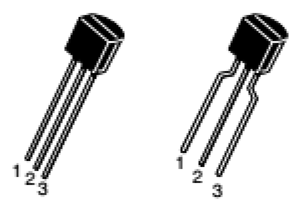
- Pb−Free Packages are Available*

ON Semiconductor®

http://onsemi.com



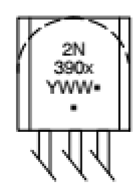
TO−92
CASE 29
STYLE 1



STRAIGHT LEAD
BULK PACK

BENT LEAD
TAPE & REEL
AMMO PACK

MARKING DIAGRAMS



x = 3 or 4
Y = Year
WW = Work Week
• = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	40	Vdc
Collector−Base Voltage	V_{CBO}	60	Vdc
Emitter−Base Voltage	V_{EBO}	6.0	Vdc
Collector Current − Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS (Note 1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	83.3	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Indicates Data in addition to JEDEC Requirements.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

2N3903, 2N3904

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

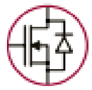
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (Note 2) (I_C = 1.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	40	–	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		$V_{(BR)CBO}$	60	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		$V_{(BR)EBO}$	6.0	–	Vdc
Base Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)		I_{BL}	–	50	nAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)		I_{CEX}	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (Note 2)		h_{FE}			–
(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	2N3903		20	–	
	2N3904		40	–	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)	2N3903		35	–	
	2N3904		70	–	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	2N3903		50	150	
	2N3904		100	300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N3903		30	–	
	2N3904		60	–	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	2N3903		15	–	
	2N3904		30	–	
Collector–Emitter Saturation Voltage (Note 2)		$V_{CE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			–	0.2	
(I_C = 50 mAdc, I_B = 5.0 mAdc			–	0.3	
Base–Emitter Saturation Voltage (Note 2)		$V_{BE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			0.65	0.85	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			–	0.95	
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain – Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N3903		250	–	
	2N3904		300	–	
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	–	4.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	–	8.0	pF
Input Impedance		h_{ie}			k Ω
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		1.0	8.0	
	2N3904		1.0	10	
Voltage Feedback Ratio		h_{re}			X 10^{-4}
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		0.1	5.0	
	2N3904		0.5	8.0	
Small–Signal Current Gain		h_{fe}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		50	200	
	2N3904		100	400	
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{oe}	1.0	40	μmhos
Noise Figure		NF			dB
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k Ω, f = 1.0 kHz)	2N3903		–	6.0	
	2N3904		–	5.0	

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Max	Unit
Delay Time	(V_{CC} = 3.0 Vdc, V_{BE} = 0.5 Vdc, I_C = 10 mAdc, I_{B1} = 1.0 mAdc)		t_d	–	35	ns
Rise Time			t_r	–	35	ns
Storage Time	(V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = I_{B2} = 1.0 mAdc)	2N3903	t_s	–	175	ns
		2N3904		–	200	
Fall Time			t_f	–	50	ns

2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

Supertex inc. **DN2535**



N-Channel Depletion-Mode Vertical DMOS FETs

Features

- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on-resistance
- Free from secondary breakdown
- Low input and output leakage

Applications

- Normally-on switches
- Solid state relays
- Converters
- Linear amplifiers
- Constant current sources
- Power supply circuits
- Telecom

General Description

The Supertex DN2535 is a low threshold depletion mode (normally-on) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

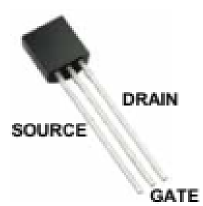
Part Number	Package Option	Packing
DN2535N3-G	TO-92	1000/Bag
DN2535N3-G P002	TO-92	2000/Reel
DN2535N3-G P003		
DN2535N3-G P005		
DN2535N3-G P013		
DN2535N3-G P014		
DN2535N5-G	TO-220	50/Tube

-G denotes a lead (Pb)-free / RoHS compliant package.
Contact factory for Wafer / Die availablity.
Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

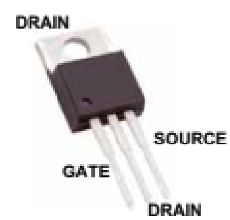
Product Summary

BV_{DSX}/BV_{DGX}	$R_{DS(ON)}$ (max)	I_{DSS} (min)
350V	25Ω	150mA

Pin Configuration



3-Lead TO-92



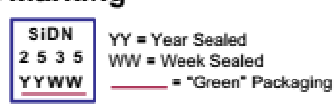
3-Lead TO-220

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSX}
Drain-to-gate voltage	BV_{DGX}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C

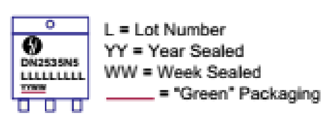
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking



Package may or may not include the following marks: Si or

3-Lead TO-92



Package may or may not include the following marks: Si or

3-Lead TO-220

Typical Thermal Resistance

Package	θ_{ja}
TO-92	132°C/W
TO-220	29°C/W

Doc.# DSFP-DN2535
B062813

DN2535

Thermal Characteristics

Package	I_D (continuous)†	I_D (pulsed)	Power Dissipation @T_C = 25°C	I_{DR}†	I_{DRM}
TO-92	120mA	500mA	1.0W	120mA	500mA
TO-220	500mA	500mA	15W	500mA	500mA

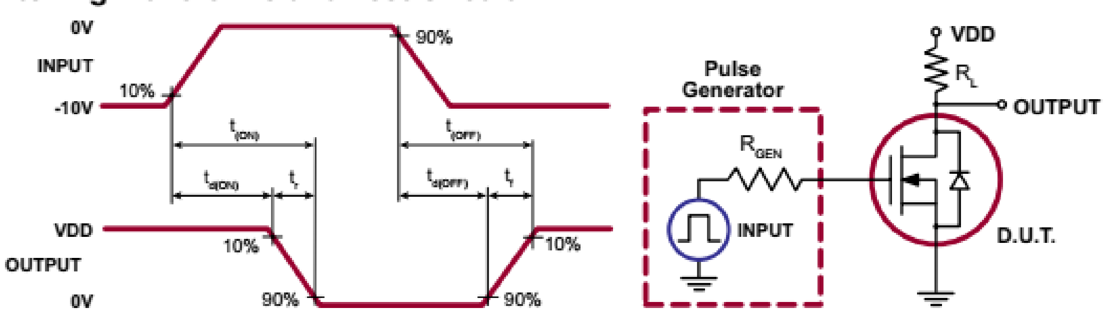
Notes:
† I_D (continuous) is limited by max rated T_j

Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSX}	Drain-to-source breakdown voltage	350	-	-	V	V_{GS} = -5.0V, I_D = 100µA
$V_{GS(OFF)}$	Gate-to-source off voltage	-1.5	-	-3.5	V	V_{DS} = 25V, I_D = 10µA
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with temperature	-	-	-4.5	mV/°C	V_{DS} = 25V, I_D = 10µA
I_{GSS}	Gate body leakage current	-	-	100	nA	V_{GS} = ±20V, V_{DS} = 0V
$I_{D(OFF)}$	Drain-to-source leakage current	-	-	10	µA	V_{DS} = Max rating, V_{GS} = -10V
		-	-	1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = -10V, T_A = 125°C
I_{DSS}	Saturated drain-to-source current	150	-	-	mA	V_{GS} = 0V, V_{DS} = 25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	17	25	Ω	V_{GS} = 0V, I_D = 120mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.1	%/°C	V_{GS} = 0V, I_D = 120mA
G_{FS}	Forward transconductance	-	325	-	mmho	V_{DS} = 10V, I_D = 100mA
C_{ISS}	Input capacitance	-	200	300	pF	V_{GS} = -10V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	12	30		
C_{RSS}	Reverse transfer capacitance	-	1.0	5.0		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	V_{DD} = 25V, I_D = 150mA, R_{GEN} = 25Ω,
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	15		
t_f	Fall time	-	-	20		
V_{SD}	Diode forward voltage drop	-	-	1.8	V	V_{GS} = -10V, I_{SD} = 120mA
t_{rr}	Reverse recovery time	-	800	-	ns	V_{GS} = -10V, I_{SD} = 1.0A

Notes:
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

Switching Waveforms and Test Circuit



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(ELECTRONICS 2)

REPORT SHEET 1

BIPOLAR JUNCTION TRANSISTOR (BJT) AND FIELD EFFECT TRANSISTOR (FET) : AC ANALYSIS

Group members	**1.**
	2.
	3.
Lecturer	**:**
Date	**:**

No.	PO	CO	Student Marks	Marks
1	PLO1	CO1		40
2	PLO2	CO2		30
3	PLO4			20
3	PLO8			10
		Total Marks		/100

EXPERIMENT 1 : BIPOLAR JUNCTION TRANSISTOR (BJT) : DC AND AC ANALYSIS

Part A : BJT AC Biasing

Measurement (Multimeter)			**Calculation**		**Measurement (Oscilloscope)**			
I_B (mA)	**I_c(mA)**	**I_E (mA)**	$r_e = \frac{26mV}{I_E}$	$A_v = \frac{-R_c}{r_e}$	**$V_{sig(peak)}$**	**$V_{o(peak)}$**	$A_v = \frac{V_o}{V_i}$	$r_e = \frac{-R_c}{A_v}$

Table 1

PLO1	CLO1	……… /10m

Sketch of V_i and V_o

PLO1	CLO1	……… /10m

Part B : BJT : Input impedance, Z_i

$\beta = \frac{I_C}{I_B}$	Z_i (from Eq.1)	$V_{sig\ (peak)}$	$V_{i(peak)}$	Z_i (from Eq.2)

Table 2

PLO1	CLO1	.... /10m

Part C : BJT : Output Impedance, Z_o

Calculation (Theory)		Measurement	
	Z_o	Output Voltage (peak)	Z_o (from Eq.3)
No load		V_O =	
With load		V_L =	

Table 3

PLO1	CLO1	.... /10m

Part D : D-MOSFET : Determination of Saturation Current, I_{DSS} and Pinch Off Voltage , Vp

I_{DSS} (mA)	V_P (V)

Table 4

PLO1	CLO1	.... /10m

Part E : D-MOSFET -AC Biasing

Measurement (Multimeter)	Calculation		Measurement (Oscilloscope)		
V_{GS} (V)	$g_m = 2\frac{I_{DSS}}{V_P}(1 - \frac{V_{GS}}{V_P})$	$A_v = -g_m R_D$	$V_{sig(peak)}$	$V_{o(peak)}$	$A_v = \frac{V_o}{V_i}$

Table 5

PLO1	CLO1	……… /10m

Questions:

Ql. Compare the voltage gain of BJT and D- MOSFET obtained using calculation and measurement. Give your comments.

………
………
………
………
………
………
………

PLO1	CLO1	……… /10m

Q2. Discuss the function of the circuits (Compare the input and output waveforms).

………
………
………
………

PLO1	CLO1	.... /10m

Q3. Compare the values of input impedance obtained using Equation 1 and Equation 2. Give your comments.

....

....

....

....

PLO1	CLO1	.... /10m

Q4. From Table 3, compare the values of output impedance. Give your comments.

....

....

....

....

PLO1	CLO1	.... /10m

Q5. Conclusion

....

....

....

....

....

PLO4		.... /10m

PLO2 (Psychomotor/Hands On Skills) for LABS Experiments

	Criteria	Very poor (5 Marks)	Poor (10 Marks)	Moderate (15 Marks)	Good (20 Marks)	Excellent (25 Marks)
1	**Ability to perform lab works based on the manual/ guidelines provided**	Not at all	Quite Limited /Selectively	Can perform lab work moderately but require a lot of guidance	Can perform lab work systematically and only need minor guidance	Demonstrate systematic and excellent performances
2	**Ability to perform simple lab work without supervision**	Need full supervision	Major supervision	Minor supervision	Limited supervision	Work independently With no supervision
3	**Ability to carry out lab work efficiently on the following criteria, (circuit assembly, using measurement apparatus and techniques)**	Not able to construct a full circuit, poor/inaccurate measurement techniques/usage of equipment	Completed full circuit but poor/inaccurate measurement techniques/usage of equipment	Completed full circuit and it works successfully. However the measurement techniques/usage of equipment had some minor deficiency	Completed full circuit and it works successfully. However the measurement techniques/usage of equipment had produced a few errors/corrections.	Circuit was completed and works properly without any errors /corrections. Also demonstrated an excellent skills/conducts.
4	**Ability to collect the required data, performs appropriate analysis and/or troubleshooting (if necessary).**	Not able to collect data and/or perform analysis	Limited data collection but not able to perform analysis/ troubleshooting	Demonstrates major errors in data collection and /or analysis. Limited ability in troubleshooting	Minor error in data collection and analysis. Good approach/techniques in troubleshooting .	Data collection and data analysis are done systematically and performs excellent approaches to trouble shoot (if necessary)

PLO4 For Laboratory Report

	Criteria	Very Poor (5 Marks)	Poor (10 Marks)	Moderate (15 Marks)	Good (20 Marks)	Excellent (25 Marks)
1	**Data Collection**	No data reported.	Data is brief and missing significant pieces of information.	Incomplete these of components of data (Both tables and Graphes): • ______Tables • ______Graphs	Only one component of data is incomplete (either table or graph). • Tables/Graphs	Data is completed properly and attributes mentioned below are observed with great care: • Tables are easy to read and units are provided. • Graphs are labeled and shown trends.
2	**Completing/Answering Questions**	Questions are not answered at all.	Attempts were made but gave wrong answer to every question.	Questions are answered without any depth and with many errors.	Questions are properly answered but with a few errors.	Questions are answered completely and correctly.
3	**Summary/Conclusion**	No conclusion or summary is/are drawn/reported	Conclusion is too brief without any reference to important pieces of information	Any two components of the conclusion/summary (mentioned) are missing : • Summary • Data • Hypothesis • Errors	Any component of the conclusion /Summary (mentioned) is missing: • Summary • Data • Hypothesis • Errors	Conclusion /Summary of these attributes below were addressed/reported properly, clearly and systematically. • experiment, • data cited • hypothesis/assumptions made • The source of errors.
4	**Report Quality**	No attention to detail evident.	Report contains many errors.	Report is good but with few spelling or grammatical errors.	Report is well written and cohesive, with a few errors	Report is very well written without any spelling or grammatical mistakes.

PLO8 for LABS Experiments

	Criteria -Understand the conducts, ethical values and socio-cultural impacts on professional norm and practice	Very poor (5 Marks)	Poor (10 Marks)	Moderate (15 Marks)	Good (20 Marks)	Excellent (25 Marks)
1	**Professional Practice (Punctuality/Follow the Rules)**	Non-Conforming/In-punctuality	Not always Conforming/ Not always punctual	Sometimes Conforming/ Sometimes punctual	Conformin g /Punctual	Always Conforming /Always Punctual
2	**Ethical Conduct/Behaviour (Trustworthy / Respectfulness)**	Does not practice	Not always practicing	Sometimes only	Mostly practicing	Always practicing
3	**Social Cultural (Racial Harmony)**	Does not observe	Not always observe	Sometimes observe	Mostly observe	Always observe
4	**Personality**	Mostly unpleasant	Not always pleasant	Moderately pleasant	Mostly pleasant	Always pleasant