UTM
UNIVERSITI
TEKNOLOGI MALAYSIA

Sekolah Pendidikan
Profesional dan
Pendidikan Berterusan
(SPACE)

JABATAN KEJURUTERAAN ELEKTRIK
PUSAT PENGAJIAN DIPLOMA (PPD), SPACE
UNIVERSITI TEKNOLOGI MALAYSIA
KUALA LUMPUR

DIGITAL ELECTRONICS LABORATORY

EXPERIMENT 1
DETERMINATION THE LOGIC LEVEL AND IMPLEMENTATION OF BOOLEAN AND DEMORGAN'S THEOREM

EXPERIMENT 1 : DETERMINATION THE LOGIC LEVEL AND IMPLEMENTATION OF BOOLEAN AND DE MORGAN'S THEOREM

OBJECTIVES:

1. Able to use digital lab trainer and logic probe.
2. Understand the concept of **logic level** in digital system and learn the fundamental **logic gates** in theory and practice.
3. Understand **Boolean Theorems** both in theory and practice and able to verify and implement Boolean Theorems in digital system.
4. Understand **De-Morgan's Theorems** both in theory and practice and able and implement De-Morgan's Theorems in digital system.
5. Understand the use of IC data sheets.

EQUIPMENTS

1. IC: 7400,7402, 7404, 7408 and 7432
2. Digital Lab Trainer Kit
3. Logic Probe
4. IC data sheets

Introduction to Digital Lab Trainer kit and logic probe

Brief discussion about the function of Digital Lab Trainer.

No	Part	Functions
1	Voltage Source	supply +5 Vdc.
2	LED Display	ON = logic HIGH (1), OFF = logic LOW (0).
3	Data Switch	logic input, position of switch indicate the logic level UP = logic HIGH (1), DOWN = logic LOW (0).
4	Pulse Switch	produce a HIGH logic when the switch is pressed.
5	Protoboard	place for build the circuit.
6	DVM Display	Digital Volt Meter.

Brief-discussion about the function of logic probe.

Logic probe is used for testing the logic level. The use of it is as follows:

1. Set the switch of logic probe to TTL or CMOS depend on the logic family.
2. The point tested must be touch carefully with the logic probe needle.
3. The LEVEL LED at logic probe indicates the logic level at the test point. If the LEVEL LED flashes a GREEN light, it means that the point is logic HIGH, Logic LOW is indicated by no light display at the LEVEL LED.

EXPERIMENTS PROCEDURES:

Part 1 : Logic Level analysis and fundamental of logic gates

1.1 Logic Level Analysis

1. Build the circuit as shows in Figure 1.1.
2. Set logic probe to TTL. Determine voltage values of $V_{H(max)}$, $V_{H(min)}$, $V_{L(max)}$ and $V_{L(min)}$ by adjusting variable resistor (R_2) and by Observing the status or logic probe whether it is ON Of OFF for corresponding voltage levels. Complete Table 1.1 in result sheet.
3. Repeat procedure 1.1.2 for CMOS.

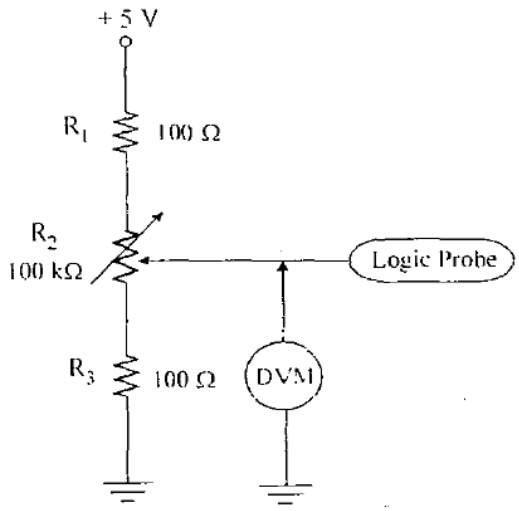

Figure 1.1

1.2 Fundamental of Logic Gates

A: IC 7404 (NOT gate)

1. Refer to Figure 1.2.1, connect A to data switch, Y to DVM. Test point Y using logic probe.
2. Complete Table 1.2.1 in result sheet. Write logic (1 or 0) in column A and Y and write the voltage reading in column Y (V).

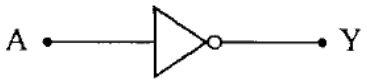

Figure 1.2.1

B: IC 7432 (OR gate)

1. Refer to Figure 1.2.2, connect A and B to data switch. Y to DVM. Test point Y using logic probe.
2. Complete Table 1.2.2.

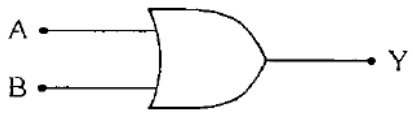

Figure 1.2.2

C: IC 7408 (AND gate)

1. Refer to Figure 1.2.3, connect A and B to data switch. Y to DVM. Test point Y using logic probe.
2. Complete Table 1.2.3.

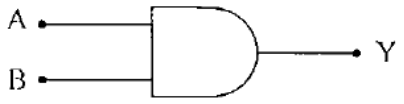

Figure 1.2.3

Part 2 : Verification of Boolean Theorems and De Morgan's theorem

2.1 Verification of Boolean Theorem

A: OR Gate

1. Built the circuit shown in Figure 2.1.1 (a), connect A to data switch and fix input (B) to ground. Test point X using logic probe or by connecting to a LED in the trainer.
2. Complete Table 2.1.1 (a). Write the status of logic probe or LED (ON or OFF).

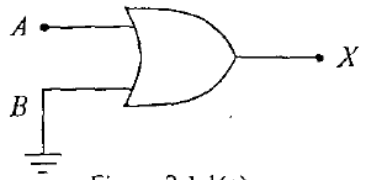

Figure 2.1.1(a)

3. Built the circuit shown in Figure 2.1.1(b), connect A to data switch and fix input (B) to +5V. Test point X using logic probe or by connecting to a LED in the trainer.
4. Complete Table 2.1.1 (b).
5. Give your brief conclusion from the result of Experiment 2.1.1 (a) and 2.1.1(b).

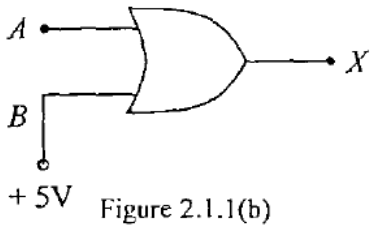

Figure 2.1.1(b)

B: AND Gate

1. Built the circuit shown in Figure 2.1.2(a), connect A to data switch and fix input (B) to ground. Test point X using logic probe or by connecting to a LED in the trainer.
2. Complete Table 2.1.2(a).

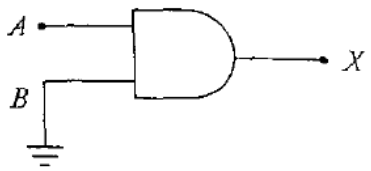

Figure 2.1.2(a)

3. Built the circuit shown in Figure 2.1.2(b), connect A to data switch and fix input (B) to +5V. Test point X using logic probe or by connecting to a LED in the trainer.
4. Complete Table 2.1.2(b).
5. Give your brief conclusion from the result of Experiment 2.1.2(a) and 2.1.2(b)

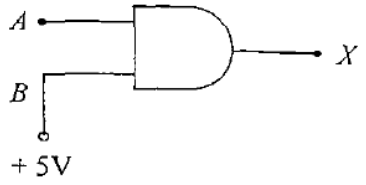

Figure 2.1.2(b)

2.2 : Verification and the use of Boolean Theorem

i. Draw a logic circuit for expression,

$$f_1(x,y,a,b) = (x + \bar{x}y) + a\bar{b}$$

ii. Complete Table 2.2.1, a truth table for f_1,

iii. Draw a logic circuit for expression f_2,

$$f_2(x,y,a,b) = x + y + a\bar{b}$$

iv. Built a circuit for expression f_2,

v. Complete Table 2.2.2, a truth table for f_2,

vi. Compare Table 2.2.2 and Table 2.2.1, and then give your conclusions from the result of Experiment Part C.

vii. Prove the equivalence of these two expressions (f_1 and f_2) using Boolean theorems.

Part 2.3 : Verification of DeMorgan's Theorems

A: Verify the equality between NOR and Negative-AND gates.

1. Refer to Figure 2.3.1 (a) and complete Table 2.3.1 (a), the truth table for NOR gate. No need to do the experiment.
2. Write the expression for *Y.*

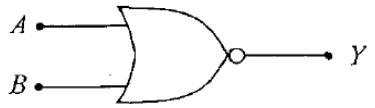

Figure 2.3.1(a)

3. Construct the circuit of Figure 2.3.1 (b). Connect *A* and *B* to data switch and monitor the output *Y* using logic probe or by connecting to LED in the trainer.
4. Complete Table 2.3.1(b).
5. Write the expression for *Y.*
6. Compare Table 2.3.1(b) and Table 2.3.1 (a), and then give your comments.

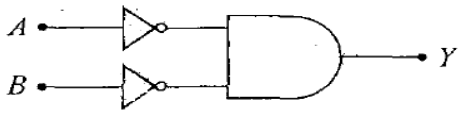

Figure 2.3.1(b)

B: Verify the equality between NAND and Negative-OR gates.

1. Refer to Figure 2.3.2(a) and complete Table 2.3.2(a), the truth table for NAND gate. No need to do the experiment.
2. Write the expression for Z.

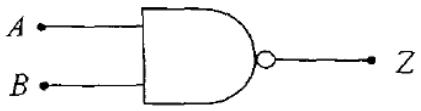

Figure 2.3.2(a).

3. Construct the circuit of Figure 2.3.2(b). Connect *A* and *B* to data switch and monitor the output Z using logic probe or by connecting to LED in the trainer.
4. Complete Table 2.3.2(b).
5. Write the expression for Z
6. Compare Table 2.3.2(b) and Table 2.3.2(a), and then give your comments.

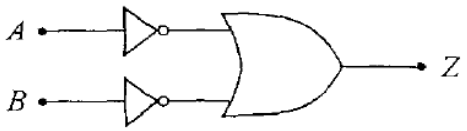

Figure 2.3.2(b)