UTM
UNIVERSITI TEKNOLOGI MALAYSIA

Sekolah Pendidikan Profesional dan Pendidikan Berterusan (SPACE)

JABATAN KEJURUTERAAN ELEKTRIK
PUSAT PENGAJIAN DIPLOMA (PPD), SPACE
UNIVERSITI TEKNOLOGI MALAYSIA
KUALA LUMPUR

DIGITAL ELECTRONICS LABORATORY

REPORT SHEET EXPERIMENT 1

Group members	**1.**
	2.
	3.
	4.
	5.
Lecturer	**:**
Date	**:**

No.	PO	CO	Student Marks	Marks
1	PLO1	CLO3		50%
2	PLO2	CLO3		30%
3	PLO4	CLO3		10%
4	PLO8	CLO5		10%
		Total Marks		/100%

EXPERIMENT 1 : DETERMINATION THE LOGIC LEVEL AND VERIFICATION OF LOGIC GATES

RESULT

Part 1.1: Logic Level analysis

Step 2: Complete Table 1.1.

Voltage value	TTL		CMOS	
	Voltage Level (DVM)	Logic Probe	Voltage Level (DVM)	Logic Probe
$V_{H(max)}$				
$V_{H(min)}$				
$V_{L(max)}$				
$V_{L(min)}$				

Table 1.1

PLO1	CLO3	.....	/4m

1.2 Fundamental of Logic Gates

A : IC 7404 (NOT gate)

Step 2: Complete Table 1.2.1.

A	Y (0 or 1)	Y(volt)

Table 1.2.1

PLO1	CLO3	.....	/2m

B : IC 7432 (OR gate)

Step 2: Complete Table 1.2.2.

A	B	Y (0 or 1)	Y(volt)

Table 1.2.2

PLO1	CLO3	.....	/4m

Part D: IC 7408 (AND gate)

Step 2: Complete Table 1.2.3.

A	B	Y (0 or 1)	Y(volt)

Table 1.2.3

PLO1	CLO3	.....	/4m

Give your brief conclusion from the result of Experiment Part 1.

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PLO1	CLO3	.....	/5m

Part 2 : Verification of Boolean Theorems and De Morgan's theorem

2.1 Verification of Boolean Theorem

A : OR Gate

A	B	X	status or logic probe (X)

Table 2.1.1(a)

PLO1	CLO3	.....	/3m

A	B	X	status or logic probe (X)

Table 2.1.1(b)

PLO1	CLO3	.....	/3m

B : AND Gate

A	B	X	status or logic probe (X)

Table 2.1.2(a)

PLO1	CLO3	.....	/3m

A	B	X	status or logic probe (X)

Table 2.1.2(b)

PLO1	CLO3	.....	/3m

Give your brief conclusion from the result of Experiment Part 2.1.

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PLO1	CLO3	.....	/5 m

2.2 : Verification and the use of Boolean Theorem

i. Draw a logic circuit for expression, $f_1(x, y, a, b) = (x + \bar{x}y) + a\bar{b}$

PLO1	CLO3	..... /2m

i. Complete Table 2.2.1, a truth table for f_1,

x	*y*	*a*	*b*	f_1

Table 2.2.1

PLO1	CLO3	..... /3m

ii. Draw a logic circuit for expression $f_2(x, y, a, b) = x + y + a\bar{b}$

PLO1	CLO3	.....	/2m

iii. Complete Table 2.2.2, a truth table for f_2,

x	*y*	*a*	*b*	f_1

Table 2.2.2

PLO1	CLO3	.....	/3m

iv. Compare Table 2.2.2 and Table 2.2.1, and then give your conclusions from the result of Experiment Part 2.2.

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PLO1	CLO3	.....	/4m

Part 2.3 : Verification of DeMorgan's Theorems

A : Verify the equality between NOR and Negative-AND gates.

A	*B*	*Y*

Figure 2.3.1(a)

Y = ……

PLO1	CLO3	…… /4m

A	*B*	*Y*	status or logic probe *(Y)*

Figure 2.3.1(b)

Y = ……

PLO1	CLO3	…… /4m

Compare Table 2.3.1(a) and Table 2.3.1(b), and then give your comments

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PLO1	CLO3	…… /4 m

Part B : Verify the equality between NAND and Negative-OR gates.

A	*B*	*Z*

Table 2.3.2(a)

Z = ……

PLO1	CLO3	…….	/4m

A	*B*	*Z*	status or logic probe *(Y)*

Figure 2.3.2(b)

Z = ……

PLO1	CLO3	…….	/4m

Compare Table 2.3.2(a) and Table 2.3.2(b), and then give your comments.

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PLO1	CLO3	…….	/10m

Give your conclusions and observation from Experiment 1.

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PLO1	CLO3	..... /20m