UTM UNIVERSITI TEKNOLOGI MALAYSIA

Sekolah Pendidikan Profesional dan Pendidikan Berterusan (SPACE)

JABATAN KEJURUTERAAN ELEKTRIK
PUSAT PENGAJIAN DIPLOMA (PPD), SPACE
UNIVERSITI TEKNOLOGI MALAYSIA
KUALA LUMPUR

DDWE 3711 ELECTRICAL ENGINEERING LABORATORY (DIGITAL INTERFACING)

EXPERIMENT 1 MEMORY

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OBJECTIVES:

To analyze and study the operation of RAM (Random Access Memory)

EQUIPMENTS:

1. Digital Lab Trainer
2. Logic Probe
3. IC 2114A (RAM) – 1 unit
4. IC 74125/74HC125 (Buffer) – 1 unit
5. IC 7475 (D-Latch)– 1 unit
6. IC 7408 (AND Gate) – 1 unit
7. IC 7404 (inverter) – 1 unit
8. Data sheet

EXPERIMENT PROCEDURE

PART A: One Memory Bit SRAM

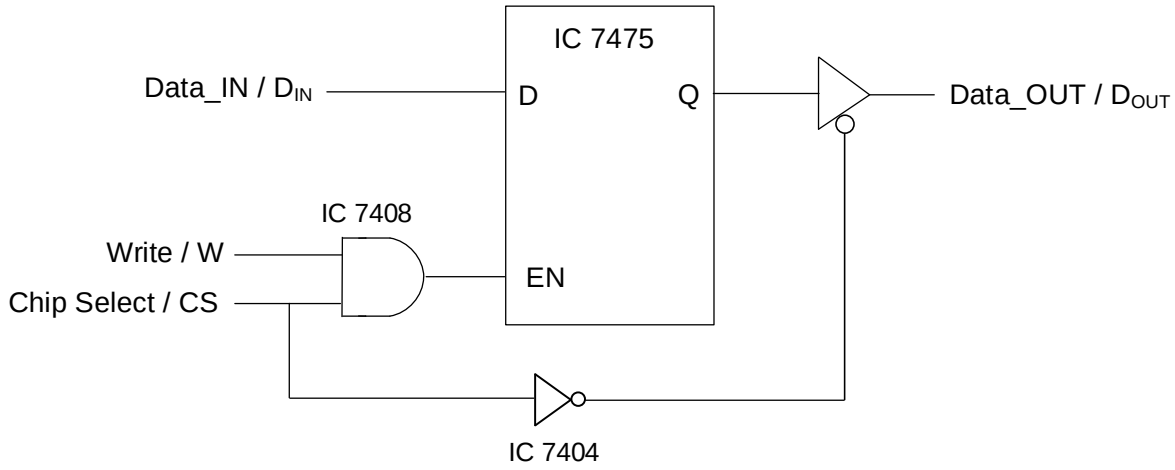


Figure 1

1. Assemble the circuit as shown in **Figure 1.**
2. Determine the output Q and Data_OUT/D_{OUT} using logic probe. The result could be **logic 1**, **logic 0** or **undetermined.**
2. Record the result in **Table 1** and answer the questions in report sheet.

PART B. RAM

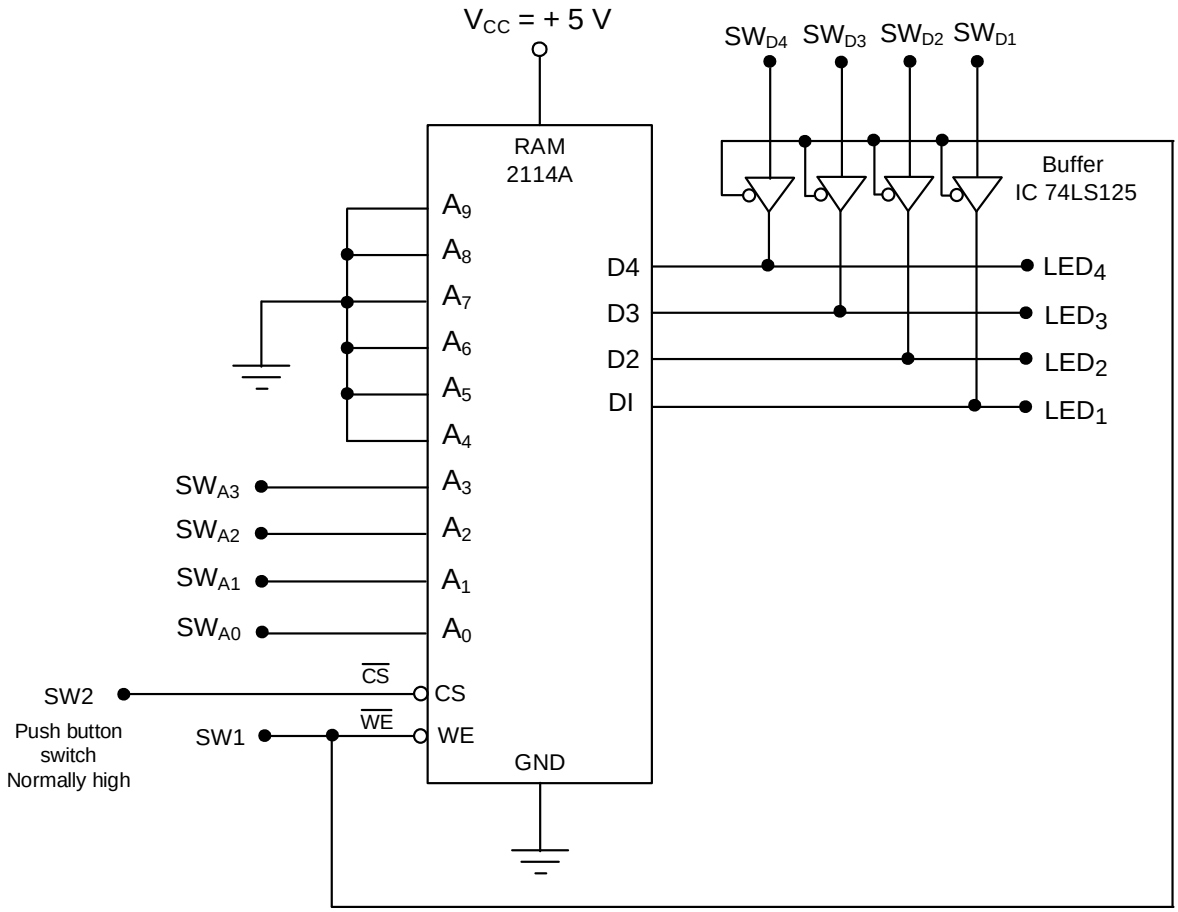
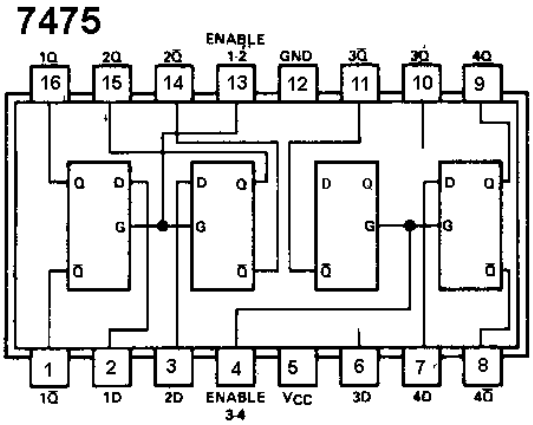
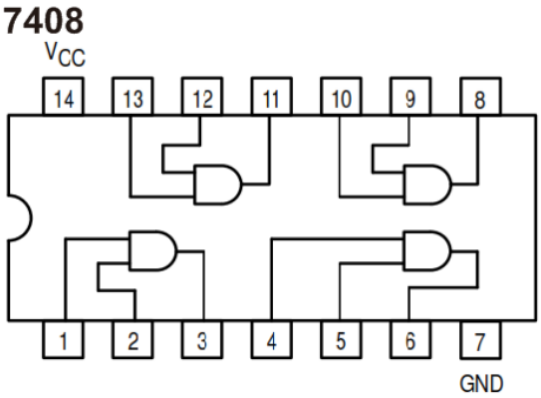


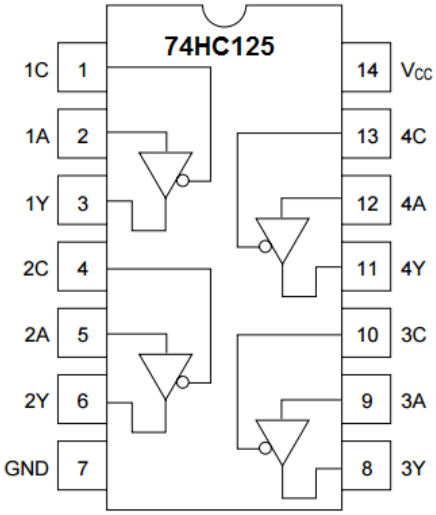
Figure 2

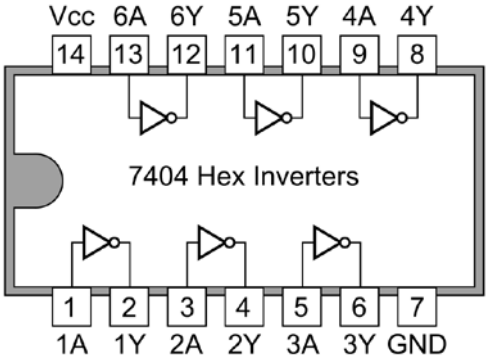
1. Assemble the circuit as shown in **Figure 2.**
2. Set the position of switch SW1, SW_{A3}, SW_{A2}, SW_{A1}, SW_{A0}, SW_{D4}, SW_{D3}, SW_{D2}, SW_{D1} as in **Table 2,** then press and release SW2. Repeat the procedure until Step_16.
2. Record the result in **Table 2** and answer the questions in report sheet.

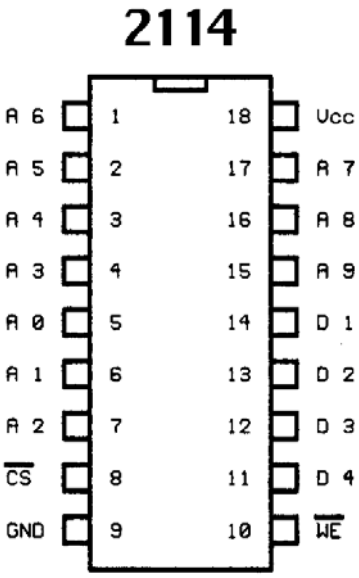
Data sheet


7475
1Q
2Q
2Q̄
ENABLE 1-2
GND
3Q̄
3Q
4Q
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
1Q̄
1D
2D
ENABLE 3-4
VCC
3D
4D
4Q̄


7408
VCC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
GND


74HC125
1C 1
1A 2
1Y 3
2C 4
2A 5
2Y 6
GND 7
14 VCC
13 4C
12 4A
11 4Y
10 3C
9 3A
8 3Y


Vcc 6A 6Y 5A 5Y 4A 4Y
14 13 12 11 10 9 8
7404 Hex Inverters
1 2 3 4 5 6 7
1A 1Y 2A 2Y 3A 3Y GND


2114
A 6 1
A 5 2
A 4 3
A 3 4
A 0 5
A 1 6
A 2 7
CS 8
GND 9
18 Vcc
17 A 7
16 A 8
15 A 9
14 D 1
13 D 2
12 D 3
11 D 4
10 WE