UTM
UNIVERSITI
TEKNOLOGI MALAYSIA

Sekolah Pendidikan
Profesional dan
Pendidikan Berterusan
(SPACE)

JABATAN KEJURUTERAAN ELEKTRIK
PUSAT PENGAJIAN DIPLOMA (PPD), SPACE
UNIVERSITI TEKNOLOGI MALAYSIA
KUALA LUMPUR

ELECTRICAL ENGINEERING LABORATORY 2

(DDWE 2701)

ELECTRONICS 1

EXPERIMENT 3

BIPOLAR JUNCTION TRANSISTOR (BJT)

AND FIELD EFFECT TRANSISTOR (FET) :

DC ANALYSIS

EXPERIMENT 3 : Bipolar Junction Transistor (BJT) and Field Effect Transistor (FET): DC Analysis.

OBJECTIVES

1. To measure DC voltages and DC currents in a common-emitter amplifier BJT .
2. To measure DC voltages and DC currents Common-source FET.

COMPONENT/EQUIPMENT

1. Function generator
2. DC Power Supply
3. BJT : 2N3904
4. D-MOSFET : DN 2535
5. Oscilloscope
6. Resistor: 1 kΩ , 3 kΩ , 10 kΩ , 390 Ω, 1 MΩ and 33 kΩ.
7. Digital Multimer
8. MicroAmmeter
9. MiliAmmeter

Part A : DC Biasing of Common Emitter BJT

Procedures:

1. Make the connections as shown in Figure 1.
2. Measure the value of I_B, I_C, I_E, V_{CE}, V_B, V_E and V_C. Complete Table 1.

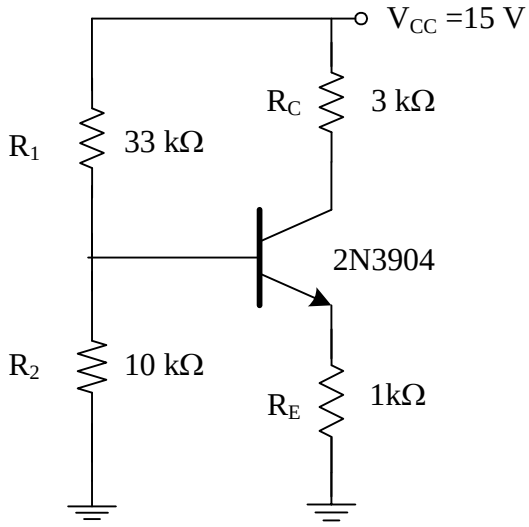


Figure 1

PART B: BJT : SWITCHING CIRCUIT

1. Construct the circuit of Figure 2
2. Apply an input ac signal, Vi = 2.5 Vp square waves. Set the frequency to 1 kHz
3. Observe Vi and Vo using oscilloscope.
4. Plot the waveforms Vo and Vi in the report sheet.

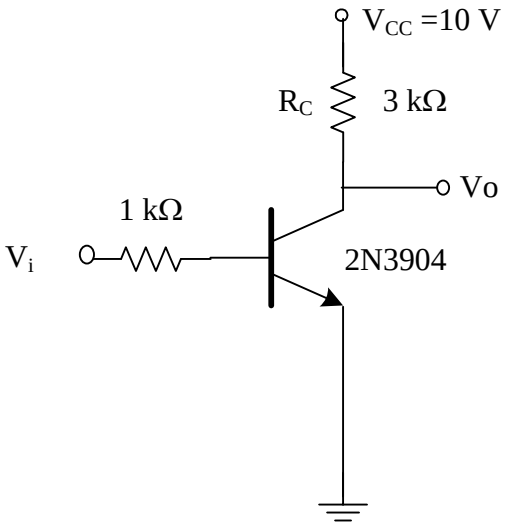


Figure 2

Part C : D-MOSFET : DETERMINATION OF SATURATION CURRENT AND PINCH OFF VOLTAGE

Procedures:

1. Make the connections as shown in Figure 3. Connect the GATE (G) to the negative voltage (V_{GG}) . This negative voltage can be obtained from the Trainer.
2. Set V_{GG} = 0 V. Measure and Record I_D in Table 2. This value is the saturation current I_{DSS}.
3. Varies V_{GG} until I_D =0 mA, Measure and Record V_{GS} in Table 2. This value is pinch off voltage, V_p

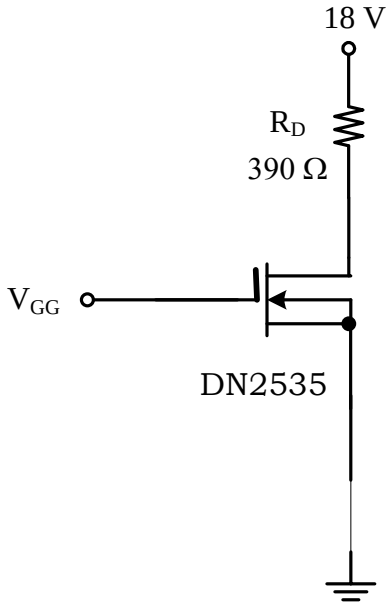


Figure 3

PART D : D-MOSFET : DC Analysis

Procedures:

1. Make the connections as shown in Figure 4.
2. Measure and record I_D, $V_{GS,}$ V_{DS}, V_D, V_S and V_G

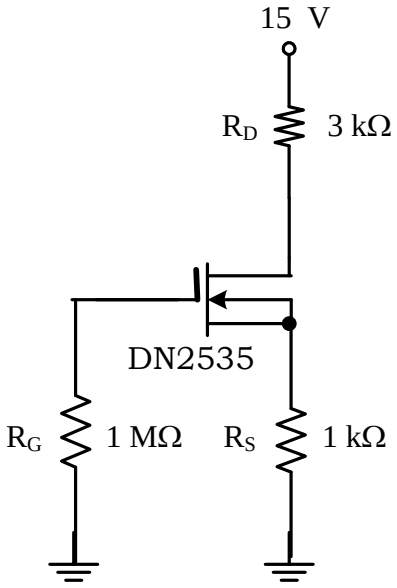


Figure 4.

2N3903, 2N3904

General Purpose Transistors

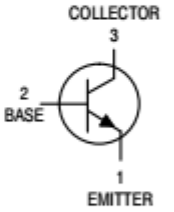
NPN Silicon

Features

- Pb–Free Packages are Available*

ON Semiconductor®

http://onsemi.com



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector – Emitter Voltage	V_{CEO}	40	Vdc
Collector – Base Voltage	V_{CBO}	60	Vdc
Emitter – Base Voltage	V_{EBO}	6.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

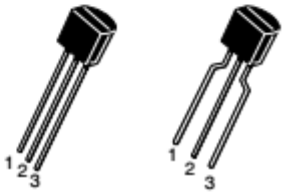
THERMAL CHARACTERISTICS (Note 1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	83.3	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Indicates Data in addition to JEDEC Requirements.

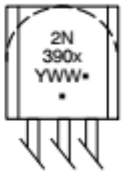
TO–92
CASE 29
STYLE 1



STRAIGHT LEAD
BULK PACK

BENT LEAD
TAPE & REEL
AMMO PACK

MARKING DIAGRAMS



x = 3 or 4
Y = Year
WW = Work Week
• = Pb–Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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2N3903, 2N3904

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (Note 2) (I_C = 1.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	40	–	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		$V_{(BR)CBO}$	60	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		$V_{(BR)EBO}$	6.0	–	Vdc
Base Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)		I_{BL}	–	50	nAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)		I_{CEX}	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (Note 2)		h_{FE}			–
(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	2N3903		20	–	
	2N3904		40	–	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)	2N3903		35	–	
	2N3904		70	–	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	2N3903		50	150	
	2N3904		100	300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N3903		30	–	
	2N3904		60	–	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	2N3903		15	–	
	2N3904		30	–	
Collector–Emitter Saturation Voltage (Note 2)		$V_{CE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			–	0.2	
(I_C = 50 mAdc, I_B = 5.0 mAdc			–	0.3	
Base–Emitter Saturation Voltage (Note 2)		$V_{BE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			0.65	0.85	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			–	0.95	
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain – Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N3903		250	–	
	2N3904		300	–	
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	–	4.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	–	8.0	pF
Input Impedance		h_{ie}			k Ω
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		1.0	8.0	
	2N3904		1.0	10	
Voltage Feedback Ratio		h_{re}			X 10^{-4}
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		0.1	5.0	
	2N3904		0.5	8.0	
Small–Signal Current Gain		h_{fe}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		50	200	
	2N3904		100	400	
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{oe}	1.0	40	μmhos
Noise Figure		NF			dB
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k Ω, f = 1.0 kHz)	2N3903		–	6.0	
	2N3904		–	5.0	

SWITCHING CHARACTERISTICS

Delay Time	(V_{CC} = 3.0 Vdc, V_{BE} = 0.5 Vdc, I_C = 10 mAdc, I_{B1} = 1.0 mAdc)	t_d	–	35	ns
Rise Time		t_r	–	35	ns
Storage Time	(V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = I_{B2} = 1.0 mAdc) 2N3903	t_s	–	175	ns
	2N3904		–	200	
Fall Time		t_f	–	50	ns

2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

Supertex inc. **DN2535**

N-Channel Depletion-Mode Vertical DMOS FETs

Features

- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on-resistance
- Free from secondary breakdown
- Low input and output leakage

Applications

- Normally-on switches
- Solid state relays
- Converters
- Linear amplifiers
- Constant current sources
- Power supply circuits
- Telecom

General Description

The Supertex DN2535 is a low threshold depletion mode (normally-on) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Part Number	Package Option	Packing
DN2535N3-G	TO-92	1000/Bag
DN2535N3-G P002	TO-92	2000/Reel
DN2535N3-G P003		
DN2535N3-G P005		
DN2535N3-G P013		
DN2535N3-G P014		
DN2535N5-G	TO-220	50/Tube

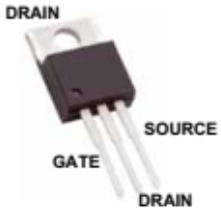
-G denotes a lead (Pb)-free / RoHS compliant package.
Contact factory for Wafer / Die availability.
Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

Product Summary

BV_{DSX}/BV_{DGX}	$R_{DS(ON)}$ (max)	I_{DSS} (min)
350V	25Ω	150mA

Pin Configuration

3-Lead TO-92



3-Lead TO-220

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSX}
Drain-to-gate voltage	BV_{DGX}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or 

3-Lead TO-92

L = Lot Number
YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or 

3-Lead TO-220

Typical Thermal Resistance

Package	θ_{ja}
TO-92	132°C/W
TO-220	29°C/W

Doc.# DSFP-DN2535
B062813

Supertex inc.
www.supertex.com